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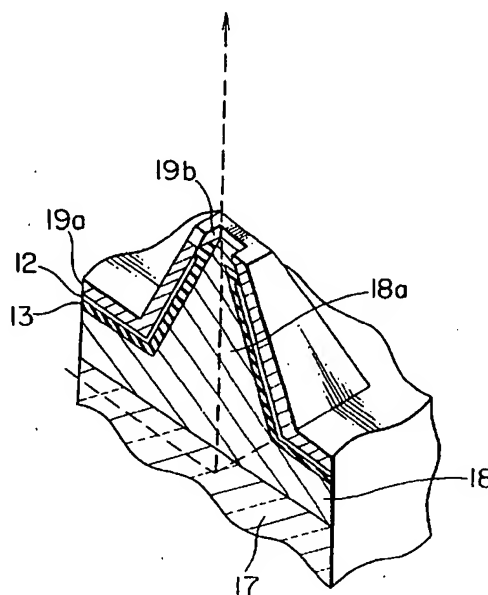
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(54) **Field emission cathode structure and method for production thereof.**

(57) A field emission cathode which comprises an emitter provided with a sharp point for emission of electrons, and a controlling gate electrode is composed of a supporting substrate (17), an emitter material layer (18) formed of an emitter material, superposed on and attached fast to the supporting substrate, and provided with an emitter hole (18a), an insulator layer (13) so formed on the surface of the emitter material layer (18) as to expose the tip part of the emitter projection (18a) therethrough, and an impurity diffusion layer (12) formed on the surface of the insulator layer (13) and enabled to function as an etching stopper layer. The method for the production of the field emission cathode comprises a step of forming a first hole (11a) pointed toward the tip thereof on a first supporting substrate (11), a step of forming the impurity diffusion layer (12) on the surface of the first supporting substrate (11), a step of forming the insulator layer (13) on the surface of the impurity diffusion layer (12), a step of depositing an emitter material layer (18) on the surface of the insulator layer including a hole while filling the hole with an emitter material thereby giving rise to a laminate, a step of integrally joining a second supporting substrate (17) to the surface of the emitter material layer (18) of the laminate, a step of removing by etching the first supporting substrate (11) thereby exposing the surface of the impurity diffusion layer (12) including the projection corresponding to the first hole (11a), and a step of selectively removing the impurity diffusion layer (12) and the insulator layer (13) thereby exposing a tip (18t) of the projection (18a) of the emitter layer (18).

**FIG. 1**



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This invention relates to a field emission cathode for use as in flat panel displays and a method for the production thereof.

In recent years, the development of field emission cathodes has come to be promoted energetically owing to the conspicuous advance of the technology for manufacture of microminiaturized LSI's. C. A. Spindt et al., for example, have disclosed in Journal of Applied Physics, Vol. 47, No 12, December 1976, pages 5248-5263 a method for the manufacture of a field emission cathode by the use of the thin-film technique and the electron beam microlithography.

The method of this kind proceeds sequentially through the steps of manufacture shown with a model in Fig. 6A, Fig. 6B, and Fig. 6C, for example. First as shown in Fig. 6A, a SiO<sub>2</sub> layer 3 is superposed on a silicon (Si) single crystal substrate 1, a gate electrode material layer 9 and a separating layer 6 are sequentially superposed further thereon, and then pin holes 4 of a diameter of about 1.5  $\mu$ m are bored through the superposed layers. Then, an emitter material 8 destined to effect field emission is formed in the form of a conical body 8a as by the vacuum deposition method on the substrate 1 as shown in Fig. 6B.

To be more specific, the SiO<sub>2</sub> layer 3 is superposed as by the CVD method and the Mo layer 9 and the Al layer 6 are further superposed sequentially as by the sputtering method on the Si single crystal substrate 1.

Subsequently, the SiO<sub>2</sub> layer 3 mentioned above, the Mo layer 9 as a gate electrode layer, and the Al layer 6 as a separating layer are selectively etched to bore a pin hole having a diameter of about 1.5  $\mu$ m as shown in Fig. 6A.

The Si single crystal substrate 1 is disposed substantially horizontally and rotated and, in the meanwhile, a material such as, for example, Mo which has the function of an emitter is vacuum deposited on the surface of the substrate from a direction perpendicular thereto as shown in Fig. 6B. In consequence of the vacuum deposition of Mo, the Mo is accumulated inside the pin hole and on the Al layer 6. Since the mouth of the pin hole 4 is gradually closed with the progress of the accumulation, the Mo is deposited in the shape of a sharply pointed cone on the substrate 1 inside the pin hole 4. Thus, a conical body 8a of Mo is obtained.

After the conical body 8a with a sharply pointed tip has been formed on the substrate inside the pin hole in consequence of the deposition of a pertinent emitter material as described above, the Mo layer 8 deposited on a gate electrode layer 9a is selectively removed and the Al layer 6 is subsequently removed to give rise to such a field emission cathode as shown in Fig. 6C.

The conventional field emission cathode described above, however, entails the following drawbacks from the practical point of view.

In the first place, the field emission cathode of the construction described above obtains the conical body 8 of an emitter material inside the pin hole 4 bored in the SiO<sub>2</sub> layer by the rotary vacuum deposition of the emitter material which makes use of the phenomenon that the mouth of the pin hole 4 gradually dwindles. The conical body 8a of the emitter material finished in the shape of a cone having a sharply pointed tip is at a disadvantage in being deficient in uniformity of field emission because the height of the conical body 8a and the shape of the tip thereof tend to be dispersed by such factors as the material and thickness of the gate electrode layer 9a, the shape and state of the pin hole 4 bored, and the conditions set for the rotary vacuum deposition. It particularly encounters the problem that the shape of the tip lacks sharpness and, therefore, the efficiency of field emission is degraded and the consumption of electric power is aggravated. Besides, the problem of the dispersion of the height of the conical body 8a and the shape of the pointed tip thereof mentioned above heavily affects the repeatability and yield of the products. When a multiplicity of field emission cathodes are manufactured on the surface of one same substrate at one same step, for example, the dispersion mentioned above entails an appreciable increase of cost.

As the second place, since the SiO<sub>2</sub> layer as a separate layer 3 is formed in a relatively large thickness as by the CVD method, the distance between the gate and the emitter greatly affects the efficiency of field emission and is not easily controlled with high accuracy. Thus, the SiO<sub>2</sub> layer 3 is deficient in uniformity of field emission and consequently susceptible of dispersion of the field emission. Generally, the field emission cathode (element) can be driven at a low voltage by closely approximating the gate and the emitter to each other. Actually, however, the efficiency of field emission is markedly dispersed and the theoretically attainable effect is not obtained because the distance between the gate and the emitter cannot be controlled with high accuracy as described above.

This invention has been produced in association with the true state of prior art described above. An object of this invention is to provide a field emission cathode which has an emitter formed uniformly in shape and has a gate separated by an accurately controlled distance from the emitter and which, therefore, generates uniform field emission, drives effectively at a low voltage, effects the field emission efficiently, and permits further integration easily.

Another object of this invention is to provide a method for producing the field emission cathode mentioned above with high efficiency enough to warrant satisfactory productivity.

The field emission cathode of this invention comprises a supporting substrate, an emitter material layer formed on the surface of the supporting substrate and provided with an emitter projection having a

sharp pointed tip, an insulator layer formed on the emitter material layer and adapted to expose the tip part of the emitter projection, and a high-concentration impurity diffusion layer formed on the insulator layer and adapted to expose the tip part of the emitter projection.

The method of this invention for the production of a field emission cathode structure comprises a step of first forming a first hole having a sharp pointed tip on a first main surface of a first supporting substrate, a step of forming a high-concentration impurity diffusion layer on the main surface of the impurity diffusion layer including the wall surfaces of the first hole, a step of forming an insulator layer on the surface the impurity diffusion layer including a second hole formed to cover the first hole, a step of forming a smooth emitter material layer surface on the surface of the insulator layer including a third hole formed to cover the second hole and meanwhile filling the third hole with an emitter material, a step of integrally joining a second supporting substrate to the surface of the emitter material layer, a step of removing by etching the first supporting substrate and exposing the impurity diffusion layer including the projection corresponding to the first hole, and a step of selectively removing the impurity diffusion layer and the insulator layer in the tip part of the projection thereby exposing the tip part of the projection formed of the emitter material.

The method otherwise is characterized by comprising a step of incising a hole having a sharp pointed bottom part on a first main surface side of a first supporting substrate, a step of forming an insulating layer on the first main surface of the first supporting substrate including the inner walls of the hole, a step of depositing an emitter material on the surface of the insulating layer while filling the emitter material in the hole thereby forming an emitter material layer provided with a projection having a sharp pointed tip, a step of joining a second supporting substrate to the surface of the emitter material layer opposite to the surface thereof on which the projection is formed thereby causing the second supporting substrate to support the emitter material layer, a step of removing by etching the first supporting substrate from the second main surface side thereof until at least the tip part of the insulating layer covering the projection of the emitter material layer is exposed, and until the end of a tip of the projection of the emitter material layer provided with the projection corresponding to the hole falls flush with the surface of the first supporting substrate after completion of the etching, and a step of progressively etching the insulating layer from the portion thereof exposed from the first supporting substrate thereby effecting selective removal by etching of the insulating layer, exposing the tip part of the projection of the emitter material layer previously covered by the insulating layer and consequently forming

an emitter and, at the same time, allowing the first supporting substrate to remain at least in such a manner as to be opposed across a gap to the tip part of the emitter and forming a gate layer.

The method is alternatively characterized by comprising a step of forming an etching stopper layer on a first main surface of a first supporting substrate, a step of incising on the first main surface side of the first supporting substrate a hole having a sharp pointed bottom part through the etching stopper layer to a depth reaching halfway along the thickness of the first supporting substrate, a step of forming an insulating layer on the etching stopper layer including the inner wall surfaces of the hole, a step of depositing an emitter material on the surface of the insulating layer while filling the emitter material in the hole thereby forming an emitter material layer provided with a projection having a sharp pointed tip, a step of removing by etching the first supporting substrate from the second main surface side of the substrate until the etching stopper layer thereby exposing the tip part of the insulating layer covering the projection of the emitter material layer through the surface of the etching stopper layer, and a step of progressively etching the insulating layer from the portion thereof exposed through the etching stopper layer thereby selectively removing by etching the insulating layer, exposing the tip part of the projection of the emitter material layer previously covered by the insulating layer and forming an emitter and, at the same time, allowing the etching stopper layer to remain at least in such a manner as to be opposed across a gap to the tip part of the emitter and forming a gate layer.

The field emission cathode of this invention has originated in the interest drawn to the fact that a pyramidal or conically hole having a sharp pointed tip can be formed on the surface of a supporting substrate such as, for example, a Si single crystal substrate by harnessing the anisotropy of etching, the fact that a layer having an impurity diffused therein functions as an etching stopper layer, the fact that the impurity diffusion layer also functions as a gate electrode layer depending on the magnitude of resistance thereof, and the fact that an oxide layer (insulator layer) having a sharp pointed tip part is formed along a prescribed surface by the use of the thermal oxidation method.

In the field emission cathode and the method for the production thereof contemplated by the present invention, the first supporting substrate may be made of any material which satisfies the condition that it should permit a hole of a sharp pointed tip to be selectively formed therein and exhibit a selective etching property with respect to an insulating layer and a high-concentration impurity diffusion layer to be integrally joined thereto. It is, however, desired to be a Si or Ge single crystal substrate in due respect of the ease with which the high-concentration impurity dif-

fusion layer is formed and the ease with which the formation of an insulator layer rich in accuracy of film thickness and shape is controlled.

Silicon (Si) containing boron (B) as a p-type impurity at a concentration of not less than  $3 \times 10^{19} \text{ cm}^{-3}$  may be cited as one example of the material for the high-concentration impurity diffusion layer. When the concentration of this impurity is as high as about  $10^{20}$  to  $10^{21} \text{ cm}^{-3}$ , the high-concentration impurity diffusion layer can be used concurrently as a gate electrode layer because the electric resistance is as low as about  $10^{-4} \Omega \cdot \text{cm}$ . It should be noted, however, that the material for the impurity diffusion layer does not need to be limited to the particular substance mentioned above. It is only required to be such that the impurity diffusion layer may function as an etching stopper layer when the first supporting substrate is removed by etching. It may be an n-type material or an i-type material instead of the p-type material mentioned above.

Further, the insulator layer may be formed by depositing  $\text{SiO}_2$  on the surface of the impurity diffusion layer mentioned above by the use of the CVD method, for example. The insulator layer, however, is desired to be formed by subjecting the surface of the impurity diffusion layer mentioned above to the process of thermal oxidation because this process imparts a dense texture to the produced layer and permits easy control of the thickness of the layer and allows the insulator layer having a sharp pointed tip to be formed along the wall surfaces of a pyramidal hole, for example.

In the method for the production of the field emission cathode according to this invention, since the high-concentration impurity diffusion layer destined to serve as an etching stopper layer and the insulator layer such as, for example, a thermally oxidized insulating layer are superposed on the surface of the first supporting substrate such as, for example, a Si single crystal substrate including the hole formed therein and the emitter material layer is subsequently superposed thereon, the thermally oxidized insulation layer can be formed as easily controlled and, therefore, the distance between the gate and the emitter can be controlled with high accuracy. Even when the insulator layer is formed in the smallest possible thickness for the purpose of closely approximating the gate and the emitter to each other, the supporting substrate can be removed by etching without exposing the insulator layer and the emitter material layer to the possibility of corrosion because the impurity diffusion layer functions as an etching stopper layer. Since the thermally oxidized insulation layer and the emitter material layer are protected against the corrosion by the etching liquid as described above and also since the distance between the gate and the emitter is decreased, the field emission efficiency and the uniformity of the field emission cathode are improved to

a great extent.

Besides, since the emitter material is disposed as embedded (filled) in the hole formed in the supporting substrate and the hole is formed with high accuracy as well, the emitter which is uniform in height, shape, and sharpness of sharp pointed tip is manufactured with high repeatability. In the hole formed in the supporting substrate, the tip of the hole gains in sharpness because the growth of the thermally oxidized insulation layer on the inner wall surfaces of the hole advances toward the interior of the hole. As a natural consequence, the tip part of the emitter formed by filling the emitter material in the hole becomes sharp (refer to Fig. 2B).

The high-concentration impurity diffusion layer primarily functions as an etching stopper layer. When it has a high p-type impurity concentration and enjoys high electric conductivity, it can be used directly as a gate electrode layer. When the etching stopper layer is concurrently used as a gate electrode layer, this layer and the insulator layer which has been formed as ideally controlled cooperate to permit accurate control of the distance between the gate and the emitter and the mutual approximation thereof and, at the same time, obviates the necessity of the step for the formation of the gate electrode layer. The omission of this step naturally results in reducing the labor, man-hour, and material cost involved in the production of the field emission cathode of this invention.

Fig. 1 is a partially sectioned perspective view showing the construction of the essential part of a field emission cathode as one embodiment of this invention.

Figs. 2A, B, C, D, E, F, G, and H are a series of model explanatory diagrams showing the first embodiment of the method for the production of a field emission cathode according to this invention.

Fig. 2A is a cross section showing the state of a hole having a sharp pointed tip formed on the surface of a supporting substrate.

Fig. 2B is a cross section showing the state of having an impurity diffusion layer, an insulator layer, an emitter material layer, and an electroconductive layer sequentially formed on the surface of the supporting substrate containing the hole.

Fig. 2C is a cross section showing the state of having an insulating supporting substrate joined in place.

Fig. 2D is a cross section showing the state of having the surface of the substrate layer removed by etching until the projection corresponding to the hole is exposed.

Fig. 2E is a cross section showing the state of having the surface including the exposed projection masked.

Fig. 2F is a cross section showing the state of having the tip of the gate electrode layer of the projection exposed.

Fig. 2G is a cross section showing the state of having the exposed tip part of the gate electrode layer removed to form an opening.

Fig. 2H is a cross section showing the state of having the tip parts of the impurity diffusion layer and the insulator layer showing through the opening of the gate electrode layer removed to expose the tip of the projection of the emitter material layer.

Figs. 3A, B, C, D, E, and F are a series of model explanatory diagrams showing the second embodiment of the method for the production of the field emission cathode according to this invention.

Figs. 4A, B, C, D, E, and F are a series of model explanatory diagrams showing the third embodiment of the method for the production of the field emission cathode according to this invention.

Figs. 5A, B, C, D, E, and F are a series of model explanatory diagrams showing the fourth embodiment of the method for the production of the field emission cathode according to this invention.

Figs. 6A, B, and C are a series of model explanatory diagrams showing the procedure for the production of a conventional field emission cathode.

Fig. 6A is a cross section showing the state of having an insulator layer incorporating therein a pin hole for the deposition of an emitter material and a gate electrode layer sequentially superposed on the surface of a Si substrate.

Fig. 6B is a cross section showing the state of having the emitter material superposed by sputtering.

Fig. 6C is a cross section showing the construction of the field emission cathode.

Now, embodiments of the present invention will be described below with reference to the accompanying drawings.

#### Embodiment 1:

The first embodiment of this invention will be described with reference to Fig. 1 and Figs. 2A, B, C, D, E, F, G, and H.

Fig. 1 is a partly sectioned perspective view schematically showing an example of the construction of a field emission cathode according to this invention. In this diagram, 17 stands for an insulating supporting substrate such as, for example, a Pyrex glass sheet, 18 for an emitter material layer superposed on the surface of the insulating supporting substrate 17 and provided integrally with a projection (main body part of the emitter) 18a pointed sharply in the tip thereof and made of an emitter material such as, for example, an emitter material layer made of such a metallic material as W, Mo, or Ta and provided with a pyramidal projection 18a having a sharp pointed tip, and 13 for an insulator layer such as, for example, a  $\text{SiO}_2$  layer covering the projection 18a of the main body of the emitter while exposing the tip part thereof. Then, 12 stands for a high-concentration im-

purity diffusion layer such as, for example, a boron (B) doped Si layer covering the surface of the insulator layer 13 while exposing the tip part of the projection 18a of the main body of the emitter and 19a for a gate electrode layer covering the surface of the impurity diffusion layer 12 while exposing the tip part of the projection 18a of the main body of the emitter.

As described above, the field emission cathode of this invention is essentially constructed by forming as the main body part of an emitter the projection 18a of an emitter material in the shape of a pyramid, for example, as superposed on the surface of the insulating supporting substrate (structural substrate) 17, then exposing the tip part of the pyramidal projection 18a in such a manner as to effect required emission of electrons in a direction substantially perpendicular to the surface of the insulating supporting substrate 17, and further disposing the electrode layer capable of functioning as a gate electrode so as to be opposed across a gap to the tip part of the projection 18a of the main body of the emitter.

The field emission cathode constructed as described above can be easily manufactured by the steps shown with a model in Figs. 2A, B, C, D, E, F, G, and H, for example.

First, a Si single crystal substrate (first supporting substrate) 11 is prepared. One main surface of this supporting substrate 11 is anisotropically etched to form a hole 11a (in the shape of an inverted pyramid) having a tip part pointed at a prescribed angle as shown in Fig. 2A.

To be more specific, a thermally oxidized film ( $\text{SiO}_2$  film) about  $0.1 \mu\text{m}$  in thickness is formed as by the dry oxidation method on the main surface of a p-type Si single crystal substrate 11 having a crystal face orientation of (100) and a resist is applied by the spin coating method to the surface of the thermally oxidized film.

Then, the resist is patterned so as to obtain an opening of the shape of the square of  $0.8 \mu\text{m}$ , for example, through the treatments of exposure and development with the aid of a stepper, the exposed area of the oxide film ( $\text{SiO}_2$  film) is selectively etched with a mixed solution of  $\text{NH}_4\text{F}$ -HF, the resist is removed, and the anisotropic etching is carried out with an aqueous 30% KOH solution to give rise to the hole 11a of the shape of an inverted pyramid  $0.56 \mu\text{m}$  in depth on the main surface of the Si single crystal substrate 11.

Subsequently, the thermally oxidized film which has served as the mask is removed with the mixed solution of  $\text{NH}_4\text{F}$ -HF and the Si layer 12 containing a P-type impurity at a concentration of not less than  $3 \times 10^{19} \text{ cm}^{-3}$  such as, for example, a B-diffused Si layer 12 having a thickness of  $0.3 \mu\text{m}$ , is superposed in a substantially uniform thickness on the surface of the Si single crystal substrate 11 containing the hole 11a of the shape of an inverted pyramid. The B-diffused Si layer 12 in this case functions as an etching stop-

per layer (sacrifice layer) during the removal of the Si single crystal substrate 11. This layer 12 can be used in its unmodified form as a gate electrode layer when the concentration of the p-type impurity is so high as to fall in the range of from  $10^{20}$  to  $10^{21}$   $\text{cm}^{-3}$  and the electric resistance is so low as to fall in the neighborhood of  $10^{-4}$   $\Omega\text{-cm}$ . In this case, the number of man-hours can be decreased and the distance between the gate and the emitter can be shortened to permit desirable mutual approximation.

Then, the Si single crystal substrate 11 provided with the p-type impurity diffusion Si layer 12 is subjected to a treatment of thermal oxidation to effect thermal oxidation of the surface of the p-type impurity diffusion Si layer 12 and give rise to the insulator layer 13 having a thickness of 0.2  $\mu\text{m}$ .

After the insulator layer 13 has been formed as described above on the surface of the p-type impurity diffusion Si layer, an emitter material such as, for example, W, Mo, or Ta is sputtered on the surface of the insulator layer 13 so as to fill the pyramidal hole covering the p-type impurity diffusion Si layer 12 and the insulator layer 13, form the emitter projection 18a conforming to the hole mentioned above, and also form the emitter material layer 18 having a smoothly finished surface and a thickness of about 0.8  $\mu\text{m}$ .

Further on the surface of the emitter material layer 18, an electroconductive layer 15 such as, for example, an ITO (indium-tin type oxide) layer 15 having a thickness of about 1  $\mu\text{m}$ , is superposed as by sputtering to produce such a laminate as shown in Fig. 2B. Here, the ITO layer 15 may be omitted, depending on the material used for the emitter material layer 18. When this omission is made, the emitter material layer 18 goes to play the part of a cathode electrode layer concurrently.

The second supporting substrate (structural substrate) such as, for example, a Pyrex glass sheet 17 having the rear surface (back surface) thereof coated with an Al layer 16 destined to serve as an electrostatic bonding electrode and having a thickness of about 0.4  $\mu\text{m}$  is superposed on the laminate mentioned above. The ITO layer 15 and the Al layer 16 are interjoined by the so-called electrostatic bonding method which resides in applying a voltage of the order of some hundreds of V between the layers (Fig. 2C). Though this union of the two layers may be accomplished by the use of an adhesive agent, the electrostatic bonding method proves more advantageous from the viewpoint of providing the produced field emission cathode with greater reduction in weight and thickness.

After the Pyrex glass sheet 17 as the structural substrate has been joined to the laminate, the rear coat (Al) layer 16 of the Pyrex glass sheet 17 is removed by etching as with a mixed acid solution of  $\text{HNO}_3\text{-CH}_3\text{COOH-HF}$ , for example.

Then, the Si single crystal substrate 11 as the

first supporting substrate is removed by etching by the use of an aqueous solution containing the mixture of ethylenediamine, pyrocatechol, and pyrazine (mixing ratio 75 cc : 12 g : 3 mg : 10 cc) to give rise to a laminate composed of the insulator layer 13 and the emitter layer 18 provided with the pyramidal projection 18a (conforming to the aforementioned pyramidal hole 11a) and covered by the p-type impurity diffusion Si layer 12 as shown in Fig. 2D. During this process of etching, the p-type impurity diffusion Si layer 12 functions as an etching stopper layer for the Si single crystal substrate 11 and discharges the role of protecting the insulator layer 13 having a small film thickness and the pyramidal projection 18a of the main body of the emitter having a sharp pointed tip against corrosion by the etching solution mentioned above.

Then, on the surface of the p-type impurity diffusion Si layer 12 which has been exposed by the removal by etching of the Si single crystal substrate 11, W is deposited in the form of a coat in a thickness of about 0.5  $\mu\text{m}$  as by the sputtering method, for example. To the surface of the W coat layer 19 formed as described above, a photoresist layer 20 is applied as by the spin coating method in a thickness such as, for example, about 0.9  $\mu\text{m}$  which is enough to conceal a tip part 19t of the projection on the surface of the W coat layer 19 embracing therein the pyramidal projection 18a of the emitter as shown in Fig. 2E.

Thereafter, by the dry etching treatment using oxygen plasma, part of the photoresist layer 20 is removed so that the tip part 19t of the projection of the W coat layer containing the projection 18a of the emitter may be exposed in a thickness of about 0.7  $\mu\text{m}$  through the surface as shown in Fig. 2F.

Subsequently, by the reactive ion etching treatment, the tip part 19t of the projection of the W coat layer 19 which has been exposed by the removal by etching of part of the photoresist layer 20 is selectively removed to form the gate electrode layer 19a provided with an opening 19b exposing the tip part of the projection covering the impurity diffusion layer 12 and the insulator layer 13 as shown in Fig. 2G.

The remainder part of the photoresist layer 20, namely the part which has functioned as a mask for the selective etching of the tip part 19t of the W coat layer, is subsequently removed. Then, the impurity diffusion layer 12 and the insulator layer 13 covering the tip part 18t of the projection 18a of the emitter are selectively removed by etching with the mixed solution of  $\text{NH}_4\text{F-HF}$  so as to expose the tip part 18t of the projection 18a of the emitter 18.

As a result, the field emission cathode is obtained which is so constructed as to expose the tip part 18t of the pyramidal projection 18a of the main body of the emitter through the opening 19b of the gate electrode layer 19a as shown in Fig. 2H.

In accordance with the method of production de-

scribed above, the high-concentration impurity diffusion layer 12 doped with an impurity is formed on the surface of the supporting substrate 11 provided with the hole formed by anisotropic etching and pointed sharply in the tip (bottom surface side) thereof, the insulator layer 13 is further formed thereon by the thermal oxidizing method, and subsequently the emitter material layer 18 is formed in such a manner as to fill the hole mentioned above. During the course of this process, the hole having a sharply pointed tip is formed in a prescribed shape with high repeatability by the anisotropic etching. Further, since the formation of the insulator layer 13 by the thermal oxidation permits growth of  $\text{SiO}_2$  of high density and since the high-concentration impurity diffusion layer 12 provides effective protection of the insulator layer 12 and the emitter material layer 18 against corrosion by etching, the emitter function part is formed which possesses a sharp pointed tip part uniform in height and shape and also excels in uniformity of quality.

Thus, the provision of field emission cathodes with stabilized quality can be realized. Further, since the insulator layer 13 can be formed in a fully accurately controlled thickness by the thermal oxidizing method, the distance between the emitter function part mentioned above and the gate electrode layer 19a (emitter-gate distance) is controlled with high accuracy. Thus, the field emission cathode is capable of operating at a relatively low voltage to effect highly efficient emission.

The embodiment described above represents a case of having the gate electrode layer 19a superposed on the surface of the impurity diffusion layer 12. The operation and effect of the embodiment under consideration are similarly attained by causing the impurity diffusion layer 12 to function as a gate electrode layer when this impurity diffusion layer 12 has a high impurity concentration and a high electric resistance or by removing the impurity diffusion layer 12 participating mainly in the selective etching of the supporting substrate 11 thereby exposing the insulator layer 13 and superposing the gate electrode layer 19a on the surface of the exposed insulator layer 13.

The effect manifested by the embodiment is invariable when the impurity mentioned above is a p-type B, Al, Ga, or In, an n-type P, As, or Ti, or an i-type Ge or Sn.

It is allowed in this invention to use as the material for the first supporting substrate such substance as GaAs in the place of Si single crystal and as the emitter material Mo, Ta, Si, or other substance having a low work function in the place of W.

The operation and effect of the present embodiment are obtained invariably when a soda glass plate is used in the place of the Pyrex glass plate as the second supporting substrate (structural substrate).

Further, the embodiment described above represents a case of handing the field emission cathode as

a unitary article. As a matter of course, a group of such field emission cathodes may be arrayed in the form of a matrix, for example, on one Si single crystal sheet to produce a planar field emission cathode.

As described above, the field emission cathode of the first embodiment of this invention has originated in the interest drawn to the fact that a pyramidal or conical hole having a pointed tip can be formed on the surface of a supporting substrate by utilizing the anisotropy of etching, the fact that a region converted into an impurity diffusion layer functions as an etching stopper layer, the fact that the impurity diffusion layer functions concurrently as a gate electrode layer when it has low resistance, and the fact that an acute oxide layer (insulator layer) is formed in a highly accurately controlled shape along a prescribed surface by the use of the thermal oxidation method. The field emission cathode of the present invention always enjoys excellent qualities of constantly displaying ideal uniformity of field emission, providing an effective operation at a low voltage, and obtaining high field emission efficiency.

Further, in accordance with the method for the production of the field emission cathode of the present invention, the field emission cathode which is endowed with such functional characteristics as mentioned above and is easily adapted for high integration can be manufactured with highly satisfactory yield and productivity (ability of quantity production). Thus, the method of production contemplated by this invention may well be rated as contributing greatly to the utilization of field emission cathodes of this type in practical applications.

#### Embodiment 2:

Figs. 3A, B, C, D, E, and F are a series of diagrams showing a process for the production of a field emission cathode as the second embodiment of this invention. The method of production according to the second embodiment will be described below with reference to these diagrams. In these diagrams, like parts found in the first embodiment are denoted by like reference numerals.

First, as shown in Fig. 3A, the Si single crystal substrate 11 offering low resistance and having a crystal face orientation of (100) is prepared as a first supporting substrate.

Then, the hole 11a sharply pointed toward the bottom part thereof is incised on one flat surface of the Si single crystal substrate 11 (hereinafter referred to as the first main surface) as shown in Fig. 3B. For the incision of the hole 11a of such a shape as described above, the method which utilizes the anisotropic etching of Si to be described hereinbelow may be adopted. To be specific, on the first main surface of the Si single crystal substrate 11 made of a Si single crystal having a crystal face orientation of (100), a



thermally oxidized film of  $\text{SiO}_2$  is superposed in a thickness of about  $0.1\ \mu\text{m}$  by the dry oxidizing method. Then, the photoresist is patterned so as to obtain an opening of the shape of the square of  $1\ \mu\text{m}$ , for example, through the treatments of exposure and development with the aid of a stepper and the thermally oxidized  $\text{SiO}_2$  film is etched by the use of the mixed solution of  $\text{NH}_4\text{F}$ -HF as an etchant. The photoresist is removed and the first main surface of the Si single crystal substrate 11 is subjected to the anisotropic etching by the use of an aqueous 30 wt% KOH solution as an etchant. As a result, the hole 11a of the shape of an inverted pyramid  $0.71\ \mu\text{m}$  in depth is incised on the first main surface side of the Si single crystal substrate 11. Then, the thermally oxidized  $\text{SiO}_2$  film remaining on the surface of the Si single crystal substrate 11 is removed by the use of the mixed solution of  $\text{NH}_4\text{F}$ -HF, for example.

Subsequently, the thermally oxidized layer 13 is formed as shown in Fig. 3C on the first main surface of the Si single crystal substrate 11 including the inner wall surfaces of the hole 11a by subjecting the surfaces mentioned above to a treatment of thermal oxidation. In the present embodiment, the thermally oxidized layer 13 is formed by the wet method of thermal oxidation so as to acquire a thickness of  $0.5\ \mu\text{m}$ . Then, on this thermally oxidized layer 13, the emitter material layer 18 using W or Mo is formed. This emitter material layer 18 is so formed as to cover the upper surface of the thermally oxidized layer 13 while filling the hole 11a. In the present embodiment, the emitter material layer 18 is deposited by the sputtering method so as to form a film  $2\ \mu\text{m}$  in thickness on the thermally oxidized layer 13 excepting the hole 11a.

Then, as a second supporting substrate, the glass substrate 17 made of such a highly heat-resistant material as Pyrex glass and provided on the rear surface thereof with the Al layer 16 of a thickness of  $0.3\ \mu\text{m}$  as a coating as shown in Fig. 3D is prepared. This glass substrate 17 is superposed on and joined fast to the surface of the emitter material layer 18 opposite to the surface thereof on which the projection 18a of a sharp pointed tip. For this union, the electrostatic bonding method may be adopted, for example. Then, the Al layer 16 on the rear surface of the glass substrate 17 is removed with the mixed acid solution of  $\text{HNO}_3$ - $\text{CH}_3\text{OOH}$ -HF.

Then, the substrate in its entirety is inverted (upside down) so that the second main surface of the Si single crystal substrate 11 opposite to the first main surface thereof may fall on the upper side and the second main surface side of the Si single crystal substrate 11 opposite to the first main surface is removed by etching by the use of the so-called EDP, i.e., a mixed aqueous solution of ethylene diamine, pyrocatechol, and pyrazine (the ratio of ethylene diamine : pyrocatechol : pyrazine : water = 75 ml : 12 g : 0.45 g : 10 ml in the present embodiment), as an etchant. In

this case, the etching time is so controlled that the Si single crystal layer 11 may remain in a thickness allowing the tip part of the projection 18a of the emitter material layer 18 to be finally exposed and, at the same time, the lower part of the emitter material layer 18 to be coated with the Si single crystal layer 11 through the thermally oxidized layer 13 as shown in Fig. 3E. Thus, the Si single crystal substrate 11 is not wholly etched evenly in the direction of thickness thereof. The Si single crystal layer 11 is used as a gate electrode. Thus, the thermally oxidized layer 13 covering the sharply pointed tip part of the projection 18a of the emitter material layer 18 is exposed from the Si single crystal layer 11.

Now, the part of the thermally oxidized layer 13 which covers the tip part of the projection 18a of the emitter material layer 18 is removed by etching with the mixed solution of  $\text{NH}_4\text{F}$ -HF as an etchant to expose the sharp pointed tip part of the projection 18a partly from the Si single crystal layer 11 as shown in Fig. 3F. Thus, the emitter is obtained.

The method of production described above has the effect of enabling the field emission cathode contemplated by this invention to be formed with ease in addition to the effect manifested by the method of production of the first embodiment.

#### Embodiment 3:

Figs. 4A, B, C, D, E, and F are a series of diagrams showing a process for the production of the field emission cathode of the third embodiment of this invention. The method of production of the third embodiment will be explained below with reference to these diagrams. In these diagrams, like parts found in the first and the second embodiment are denoted by like reference numerals.

The present embodiment is characterized by superposing the etching stopper layer 12 having boron (B) diffused therein at a high concentration and having a small thickness on the Si single crystal substrate 11 and causing the advance of the etching of the Si single crystal substrate 11 from the second main surface side thereof to be stopped by this etching stopper layer 12. It, therefore, finds no use for such complicate control of the etching time as is encountered in the second embodiment and facilitates the formation of the field emission cathode of this invention to a greater extent.

First, the etching stopper layer 12 of a small thickness is formed on the first main surface of the Si single crystal substrate 11 having a crystal face orientation of (100) by diffusing on the surface mentioned above the ions of such an impurity as boron (B) at a high concentration of not less than  $10^{19}\ \text{cm}^{-3}$ , for example. This high-concentration impurity diffusion is effected by the thermal diffusion method or the ion injection method, for example.



Then, as shown in Fig. 4B, the hole 11a pointed sharply toward the bottom part thereof is incised in the Si single crystal substrate 11 from the etching stopper layer 12 (first main surface) side in the same manner as in the first embodiment. For the incision of this hole 11a, the method which resorts to the anisotropic etching of Si may be adopted similarly to the second embodiment. To be specific, the treatment of thermal oxidation by the dry method is performed on the surface of the etching stopper layer 12 to form a thermally oxidized  $\text{SiO}_2$  film in the etching stopper layer 12 to a depth of about  $0.1 \mu\text{m}$ . The photoresist (not shown) is further applied to the thermally oxidized  $\text{SiO}_2$  film by the spin coating method. Then, the photoresist is patterned as by the treatments of exposure and development by the use of a stepper, for example, so as to obtain an opening in the shape of the square of  $1 \mu\text{m}$ . The thermally oxidized  $\text{SiO}_2$  film is subsequently patterned by the use of the mixed solution of  $\text{NH}_4\text{F}$ -HF as an etchant. Then, the photoresist mentioned above is removed and the anisotropic etching is carried out with the pattern of the thermally oxidized  $\text{SiO}_2$  film as an etching mask and the aqueous 30 wt% KOH solution as an etchant. Thus, in the etching stopper layer 12, the hole 11a having the shape of an inverted pyramid is incised in a depth of  $0.71 \mu\text{m}$  reaching beyond the first main surface of the Si single crystal substrate 11. Then, the thermally oxidized  $\text{SiO}_2$  film remaining on the surface of the etching stopper layer 12 is removed by the use of the mixed solution of  $\text{NH}_4\text{F}$ -HF, for example.

Here, an ideal etching speed is obtained even when the etching stopper layer 12 is formed on the Si single crystal substrate 11 because the aqueous KOH solution manifests a practically equal etching rate on the etching stopper layer 12 having boron (B) diffused at a high concentration therein and the Si single crystal. Even when the etching stopper layer 12 is formed on the Si single crystal substrate 11 as in the present embodiment, therefore, the hole 11a can be ideally incised. Naturally, some other etchant may be used herein on the condition that it should be capable of etching the etching stopper layer 12.

Then, the treatment of thermal oxidation is performed on the wall surfaces of the etching stopper layer 12 and the Si single crystal substrate 11 which are exposed through the hole 11a and on the flat surface of the etching stopper layer 12 to form the thermally oxidized layer 13. During the course of the thermal oxidation, the etching stopper layer 12 gains in thickness. The thickness of the etching stopper layer 12 is set preparatorily during the formation of the Si single crystal substrate 11 so that the part of the thermally oxidized layer 13 covering the tip part of the pyramidal projection 18a may protrude from the etching stopper layer 12 even after the etching stopper layer 12 is inflated as described above. Then, in the same manner as in the second embodiment described

above, such a material as W or Mo which makes an ideal emitter material is deposited on the thermally oxidized layer 13 to give rise to the emitter material layer 18.

Now, similarly to the second embodiment, the glass substrate 17 made of such a highly heat-resistant material as Pyrex glass and provided on the rear surface thereof with the Al layer 16 having a thickness of  $0.3 \mu\text{m}$  as a coating is prepared as shown in Fig. 4D. This glass substrate 17 is superposed on and attached fast to the surface of the emitter material layer 18 opposite to the surface thereof on which the pyramidal hole 18a pointed toward the tip thereof is formed. For this union, the electrostatic bonding method may be adopted similarly to the second embodiment. Then, the Al layer 16 on the rear surface of the glass substrate 17 is removed with the mixed acid solution of  $\text{HNO}_3$ - $\text{CH}_3\text{OOH}$ -HF.

Then, as shown in Fig. 4E, the Si single crystal substrate 11 is removed by etching from the second main surface side opposite to the first main surface by the use of the so-called EDP, i.e. a mixed aqueous solution of ethylene diamine, pyrocatechol, and pyrazine (the ratio of ethylene diamine : pyrocatechol : pyrazine : water = 75 ml : 12 g : 0.45 g : 10 ml in the present embodiment), as an etchant.

Here, since the etching stopper layer 12 is formed of a Si material having boron (B) diffused at a high concentration, the etchant like EDP which is used in the second embodiment manifests a considerably lower etching rate on the etching stopper layer 12 than on the single crystal of Si. As a result, the etching advancing in the Si single crystal substrate 11 from the second main surface side thereof is stopped by the etching stopper layer 12, with the result that the etching stopper layer 12 will remain practically intact. Thus, the thermally oxidized layer 13 covering the sharp pointed tip part of the projection 18a of the emitter material layer 18 can be partly exposed from the etching stopper layer 12.

Then, as shown in Fig. 4F, the part of the thermally oxidized layer 13 covering the tip part of the projection 18a of the emitter material layer 18 is removed by etching with the mixed solution of  $\text{NH}_4\text{F}$ -HF as an etchant to obtain partial exposure of the sharp pointed tip part of the projection 18a through the etching stopper layer 12. Thus, the emitter is obtained.

Incidentally, since the etching stopper layer 12 is formed of a Si material having boron (B) diffused therein at a high concentration and consequently enjoys high electric conductivity, it may be left in its unmodified form and used as a gate electrode.

The method of production of the third embodiment described above obviates the necessity of ensuring complicate control of the etching depth during the etching of the Si single crystal substrate 11 from the second main surface side thereof as involved in the second embodiment. It, therefore, brings about

the effect of enabling the field emission cathode to be formed with further increased ease in addition to the effects obtained by the methods of production of the first and the second embodiment.

#### Embodiment 4:

Figs. 5A, B, C, D, E, and F are a series of diagrams showing a process for the production of the field emission cathode of the fourth embodiment of this invention. The method of production of the fourth embodiment will be explained with reference to these diagrams. In these diagrams, like parts found in the first and the second embodiment are denoted by like reference numerals. This fourth embodiment will be described below with emphasis centering on the characteristic parts thereof which differentiate this embodiment from the embodiments described above.

The method of production of the present embodiment is characterized by using an etching stopper layer 12a formed of an n-type Si material in the place of the etching stopper layer 12 of the third embodiment described above and causing the etching advancing in the Si single crystal substrate 11 from the second main surface to be stopped by applying a reverse voltage to the etching stopper layer 12a.

First, as shown in Fig. 5A, the Si layer 12a is formed in a small thickness as by the thermal diffusion method or the ion injection method on the Si single crystal substrate 11 made of a p-type Si single crystal having a crystal face orientation of (100) and the Si single crystal substrate 11 and the Si layer 12a are joined by the pn junction across the interface.

The subsequent steps shown in Figs. 5B through 5D are practically the same as the corresponding steps used in the third embodiment described above.

The present embodiment is then characterized by adopting the electrochemical etching method at the step of removing the Si single crystal substrate 11 shown in Fig. 5E.

This method resides in applying reverse voltage to the pn junction produced in the interface between the etching stopper layer 12a and the Si single crystal substrate 11 in an aqueous KOH solution, for example, thereby selectively etching the p-type Si single crystal substrate 11 exclusively and allowing the n-type Si layer 12a to remain intact in spite of the etching.

Thus, the Si single crystal substrate 11 is progressively etched from the second main surface side thereof until the Si single crystal substrate 11 is corroded out practically throughout the entire thickness thereof and only the tip part of the projection 18a of the emitter material layer 18 is exposed through the etching stopper layer 12a.

The steps which follow are identical to the corresponding steps involved in the embodiments described above. Specifically, the part of the thermally oxidized layer 13 covering the tip part of the projection

18a of the emitter material layer 18 is removed by etching with the mixed solution of  $\text{NH}_4\text{F}$ -Hf as an etchant as shown in Fig. 5F. Thus, the sharp pointed tip part of the projection 18a is partly exposed through the Si single crystal layer 12a. The emitter is obtained as a result.

Similarly to the embodiments described above, the fourth embodiment under consideration offers the method of production which enables the gap between the emitter and the gate electrode to be formed accurately and easily.

In the second and the fourth embodiment described thus far, the etching stopper layer 12 having boron (B) diffused therein at a high concentration or the n-type Si layer 12a may be preparatorily formed by epitaxial growth on the first main surface of the Si single crystal substrate 11 at the step of Fig. 4A or Fig. 5A.

Naturally, the materials for the component layers, the formation of the layers in the form of film, the method of patterning, and the like may be variously altered without departing from the spirit of the present invention.

As clearly described in detail above, this invention has been perfected for the purpose of realizing the fact that a pyramidal or conical hole pointed toward the tip thereof can be formed in a supporting substrate by utilizing the anisotropy of etching, the fact that a region converted into an impurity diffusion layer functions as an etching stopper layer, the fact that this impurity diffusion layer functions concurrently as a gate electrode layer depending on the magnitude of resistance thereof, and the fact that an acute oxide layer (insulator layer) can be formed accurately along prescribed surfaces by utilizing the thermal oxidation method.

The field emission cathode according to this invention is endowed with excellent qualities of constantly manifesting ideal field emission uniformly, operating effectively even at a low voltage, and obtaining high efficiency in field emission. Then, the method of this invention for the production of a field emission cathode allows field emission cathodes which are furnished with such functional characteristics as mentioned above and are readily adapted for further integration to be manufactured in a highly satisfactory yield with an ability of quantity production (mass production).

#### Claims

1. A field emission cathode structure comprising an emitter provided with a sharp pointed tip for emission of electrons and a controlling gate electrode, characterized by being composed of a supporting substrate (17), an emitter material layer (18) made of an emitter material, provided with a pro-

- jection (18a), and formed on said supporting substrate, an insulator layer (13) formed on the surface of said emitter material layer (18) so as to expose a tip of said projection (18a) therethrough, and an impurity diffusion layer (12) formed on the surface of said insulator layer (13) and enabled to function as an etching stopper layer.
2. A field emission cathode structure according to claim 1, wherein said impurity diffusion layer (12) is a gate electrode layer.
  3. A field emission cathode according to claim 1, which further comprises a gate electrode layer (19a) formed on the surface of said impurity diffusion layer (12) and along the contour of said projection (18a) of said emitter material layer (18) and provided with an opening (19b) encircling said tip of said projection (18a).
  4. A field emission cathode according to claim 1, wherein said supporting substrate (17) is a glass plate.
  5. A field emission cathode according to any of claims 1 to 4, wherein said impurity diffusion layer (12) is a silicon layer containing a p-type impurity.
  6. A field emission cathode according to any of claims 1 to 5, wherein said p-type impurity is boron (B) and is diffused at a concentration of not less than  $3 \times 10^{19} \text{ cm}^{-3}$ .
  7. A field emission cathode according to any of claims 1 to 6, wherein said impurity diffusion layer (12) has electric resistivity of not more than  $10^{-3} \Omega \cdot \text{cm}$ .
  8. A field emission cathode according to any of claims 1 to 7, wherein said insulator layer (13) is a thermally oxidized insulating layer formed of  $\text{SiO}_2$ .
  9. A method for the production of a field emission cathode structure comprising an emitter provided with a sharp point for emission of electrons and a controlling gate electrode, characterized by comprising a step of forming a first hole (11a) having a sharp pointed tip on a first (supporting) substrate (11), a step of forming an impurity diffusion layer (12) on the surface of said first (supporting) substrate (11) including said first hole (11a), a step of forming an insulator layer (13) on the surface of said impurity diffusion layer (12) including said hole, a step of depositing an emitter material layer (18) on the surface of said insulator layer (13) including said hole while filling said hole with the emitter material, a step of integrally joining a second substrate (17) to the surface of said emitter material layer (18), a step of removing by etching said first substrate (11) thereby exposing the surface of said impurity diffusion layer (12) provided with a projection (18a) corresponding to said first hole (11a), and a step of selectively removing said impurity diffusion layer (12) and said insulator layer (13) thereby exposing a tip (18t) of the projection (18a) of said emitter material layer (18).
  10. A method according to claim 9, wherein said impurity diffusion layer (12) is formed as a gate electrode layer.
  11. A method according to claim 9, which further comprises a step of forming a gate electrode layer (19a) on the surface of said impurity diffusion layer (19) after the step of removing by etching said first supporting substrate (11) thereby exposing the surface said impurity diffusion layer (19) provided with a projection corresponding to said first hole (11a) and the step of selectively removing said impurity diffusion layer (12) and said insulator layer (13) thereby exposing the tip (18t) of the projection (18a) of said emitter material layer (18).
  12. A method according to any of claims 9 through 11, wherein the integral union of said emitter material layer (18) and said second supporting substrate (17) is carried out by the electrostatic bonding method.
  13. A method according to any of claims 9 through 12, wherein the formation of said insulator layer (13) is effected by thermally oxidizing said impurity diffusion layer (12).
  14. A method according to any of claims 9 through 13, wherein said impurity diffusion layer (12) is formed by doping at least one element selected from the group consisting of B, Al, In, P, As, Ti, Ge, and Sn as an impurity into Si.
  15. A method according to claim 14, wherein the concentration of said impurity is not less than  $3 \times 10^{19} \text{ cm}^{-3}$ .
  16. A method for the production of a field emission cathode comprising an emitter provided with a sharp point for emission of electrons and a controlling gate electrode, characterized by comprising a step of forming a hole (11a) having a sharp point on a first supporting substrate (11), a step of forming an insulator layer (13) on the surface of said first supporting substrate (11) including

said hole (11a), a step of depositing an emitter material layer (18) on the surface of said insulator layer including said hole while filling said hole with an emitter material, a step of integrally joining said second supporting substrate (17) to the surface of said emitter material layer (18), a step of etching said first supporting substrate (11) through the exposed surface thereof until the end of a tip (18t) of the projection (18a) of said emitter material layer (18) provided with the projection (18a) corresponding to said first hole (11a) falls flush with the surface of said supporting substrate (11) after completion of said etching, and a step of selectively removing said insulator layer (13) thereby exposing the tip (18t) of the projection (18a) of said emitter material layer (18).

17. A method for the production of a field emission cathode comprising an emitter provided with a sharp point for emission of electrons and a controlling gate electrode, characterized by comprising a step of forming an etching stopper layer (12) on the first main surface of a first supporting substrate (11), a step of forming a hole (11a) having a sharp pointed tip on said first main surface side of said supporting substrate (11) through said etching stopper layer (12) to a depth reaching halfway along the thickness of said first supporting substrate (11), a step of forming an insulator layer (13) on the surface of said etching stopper layer (12) including said hole (11a), a step of depositing an emitter material layer (18) on the surface of said insulator layer (13) including the hole while filling said hole with an emitter material, a step of integrally joining a second supporting substrate (17) to the surface of said emitter material layer (18), a step of removing by etching said first supporting substrate (11) from a second main surface side thereof until said etching stopper layer (12) thereby exposing an end part of said insulator layer (13) of a protruding part of corresponding said hole (11a), and a step of selectively removing said insulating layer thereby exposing a tip (18t) of a projection (18a) of said emitter material (18).

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FIG. 1

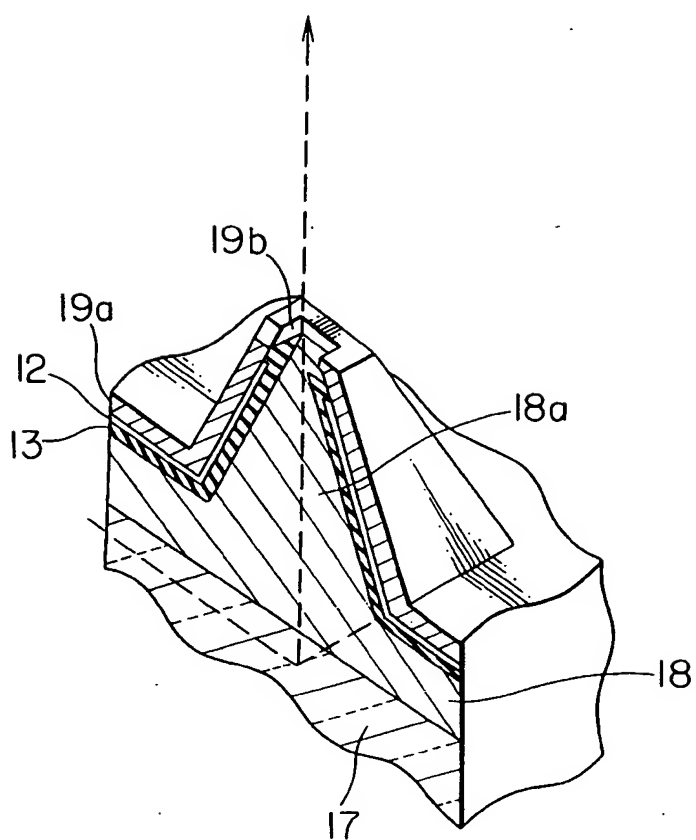


FIG. 2A

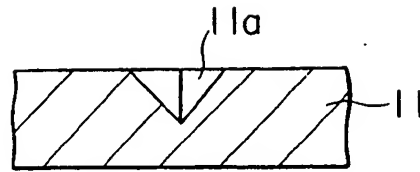


FIG. 2B

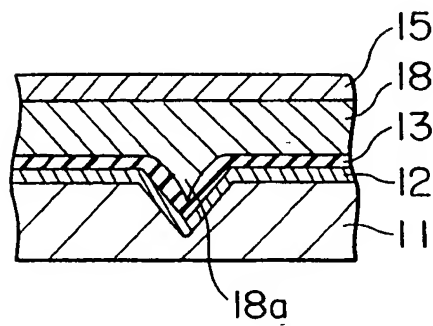


FIG. 2C

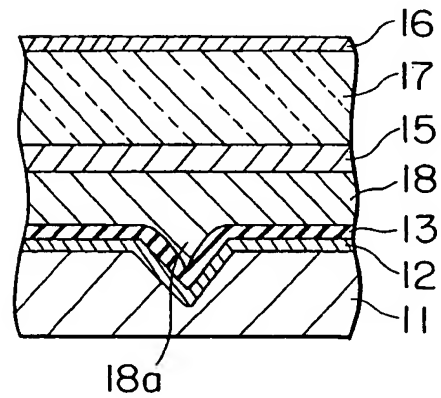


FIG. 2D

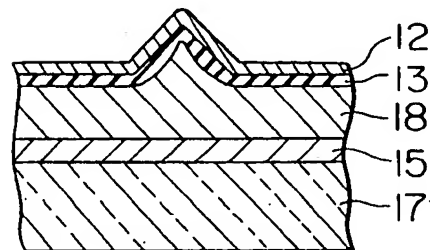


FIG. 2E

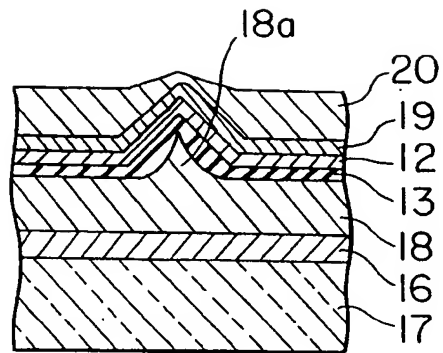


FIG. 2F

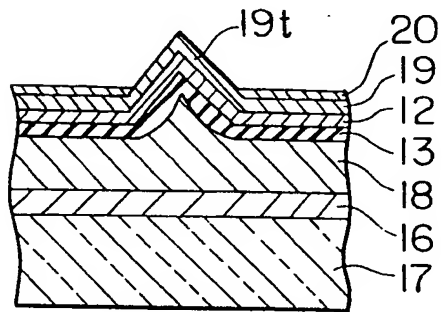


FIG. 2G

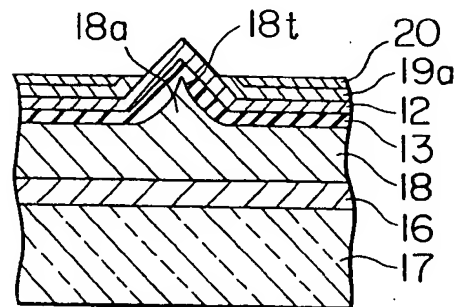


FIG. 2H

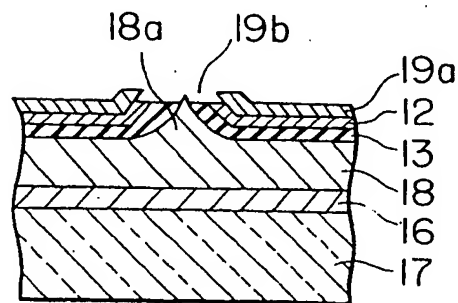




FIG. 3A

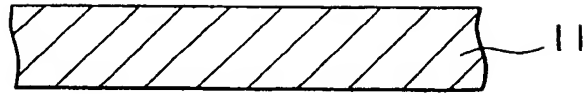


FIG. 3B

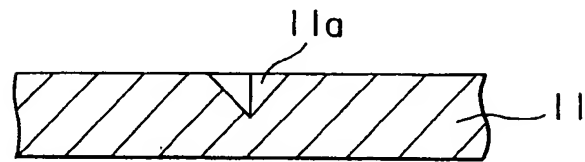


FIG. 3C

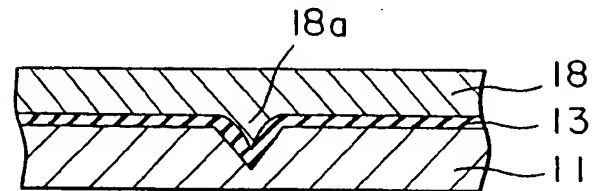


FIG. 3D

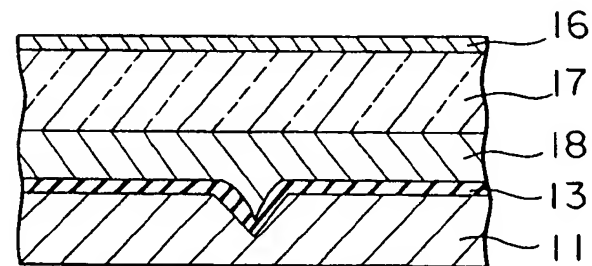


FIG. 3E

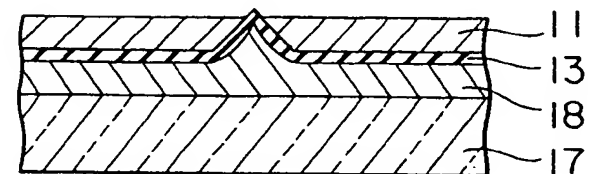


FIG. 3F

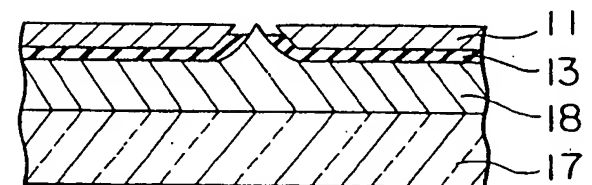


FIG. 4A

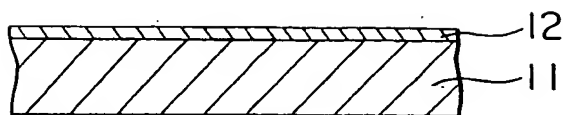


FIG. 4B

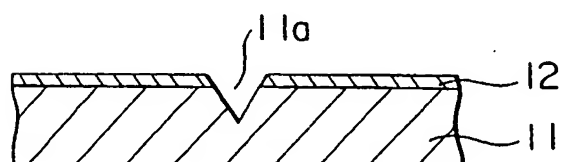


FIG. 4C

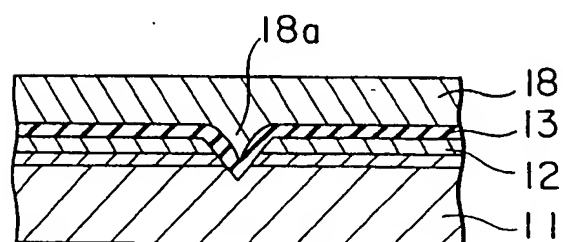


FIG. 4D

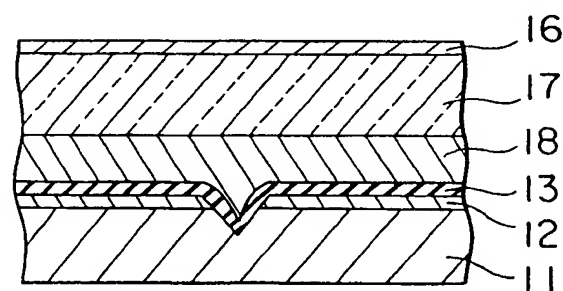


FIG. 4E

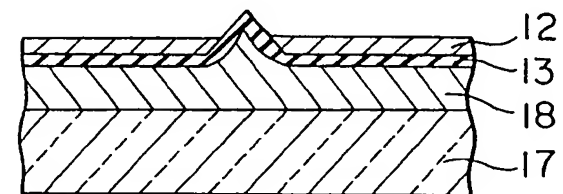


FIG. 4F

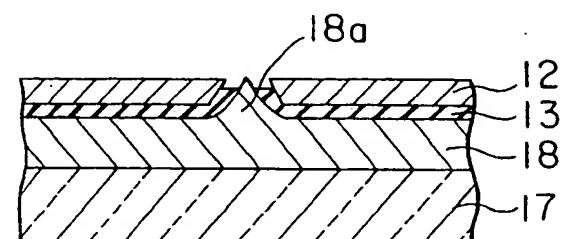


FIG. 5A

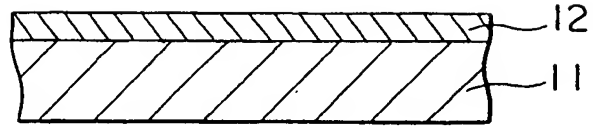


FIG. 5B

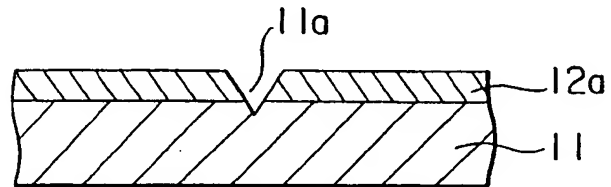


FIG. 5C

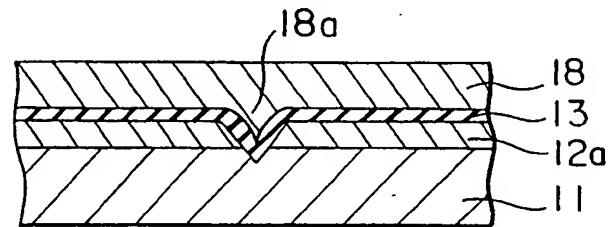


FIG. 5D

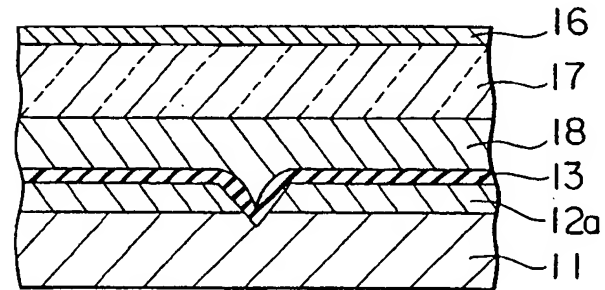


FIG. 5E

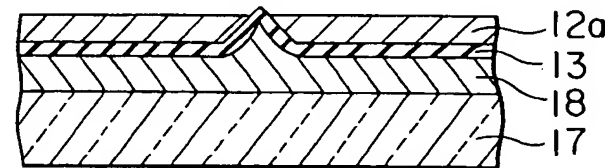


FIG. 5F

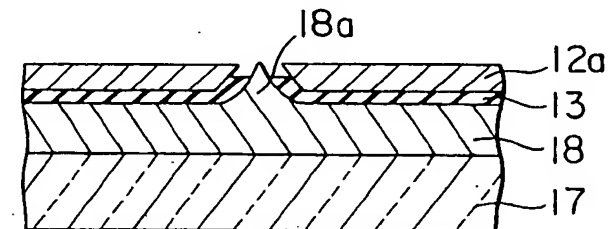


FIG. 6A

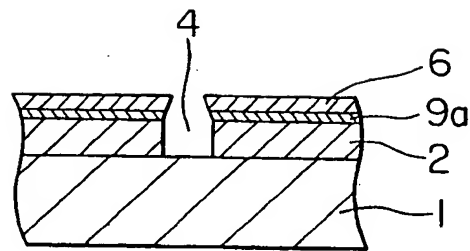


FIG. 6B

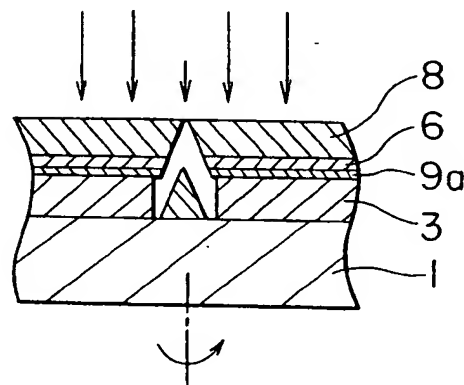
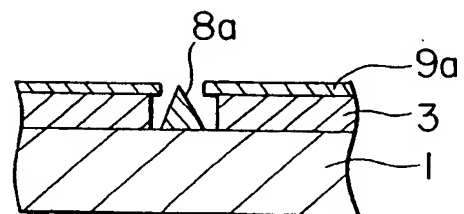


FIG. 6C





European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 94 30 6076

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	FR-A-2 657 999 (MITSUBISHI DENKI KK) * claims 1-9 *	1,9	H01J1/00 H01J1/30 H01J9/02
P,A	DE-A-43 10 604 (KK TOSHIBA) * claims 1-12 *	9	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H01J
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 12 December 1994	Examiner Van den Bulcke, E
<p><b>CATEGORY OF CITED DOCUMENTS</b></p> <p>X : particularly relevant if taken alone  Y : particularly relevant if combined with another document of the same category  A : technological background  O : non-written disclosure  P : intermediate document</p> <p>T : theory or principle underlying the invention  E : earlier patent document, but published on, or after the filing date  D : document cited in the application  L : document cited for other reasons  &amp; : member of the same patent family, corresponding document</p>			

EPM TC 2800

FINAL SEARCH DATE 12/01/03

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